

AT-1120 / AT-1212

High Speed Arbitrary Signal Generator



14 Bit - 2 GS/s Real Time Sample Rate

800 MHz Analog Bandwidth

Customizable FPGA & Digital Signal Processing

Multiple Module Synchronization: up to 32 CH

AT-1120 / AT-1212

WIDEBAND, HIGH RESOLUTION ARBITRARY WAVEFORMS

**HIGH SPEED MODULAR SIGNAL GENERATOR:
2 GS/s REAL TIME SAMPLE RATE - 800 MHz ANALOG BANDWIDTH**

NEW GENERATION WAVEFORMS FOR COMPLEX REAL-WORLD SIGNALS

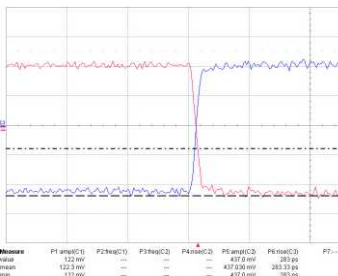
High bandwidth and high resolution AWGs help you to generate with confidence complex signals like digital modulations and RF stimuli for functional and performance tests.

AT-1120/AT-1212 FlexRIO Modules, by combining up to 2 GS/s with 14 Bit Vertical Resolution, generate high performance analog waveforms to meet demanding for test signals and applications where speed, resolution and quality is an issue.

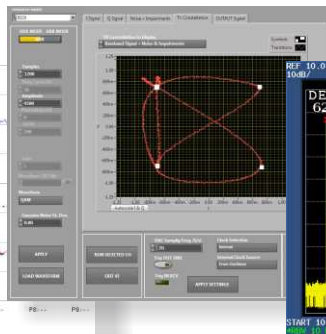


- RF Signal Generation
- Digital Modulations
- Extended waveform memory by using FlexRio onboard DRAM
- Very Low Harmonic Distortion
- Arbitrary and DDS modes
- Real Time Data Streaming and Processing
- LabView FPGA Graphical Programming

Impulse Response



Customizable LabView SW



Signal Fidelity



AT-1120 KEY FEATURES*



- 2 GS/s Sample Rate
- 14 Bit Resolution
- 1 Channel
- 800 MHz Analog Bandwidth
- DC Coupled Output:
2 Vpp Differential / 1 Vpp S.E.
- Harmonic distortion:
< -65 dBc
- Non-harmonic spurious:
< -75 dBc (1kHz to 800 MHz)

AT-1212 KEY FEATURES*



- 1.25 GS/s Sample Rate
- 14 Bit Resolution
- 2 Channels
- 480 MHz Analog Bandwidth
- DC Coupled Output:
4 Vpp Differential / 2 Vpp S.E.
- Harmonic distortion:
< -65 dBc
- Non-harmonic spurious:
< -75 dBc (1 KHz to 480 MHz)

*Preliminary. Subject to change without notice.

About Active Technologies

Active Technologies is an Italian company expert in semiconductor test equipment and electronic instrumentation design. The company offers custom design and manufacturing services (OEM/ODM) taking advantage of its skills on high performance test instrumentation development.

Active Technologies has partnerships with companies world leader in T&M like LeCroy, Tektronix and National Instruments.

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SPECIFICATIONS

AT1120 FlexRIO Adapter Module

Specifications		
Number of Analog Channels	1	
DAC Resolution	14 Bit	
Sampling Rate	2 GS/s	
DC-coupled analog output		
Characteristics	DC Output	
Output type	Single ended or differential	
Impedance	50 Ω / 100 Ω	
Amplitude¹ , 50 Ω Load (1KHz sine wave) Full Scale Range, Single Ended Full Scale Range, Differential Resolution	1 Vp-p (1.1Vpp without calibration) 2 Vp-p (2.2 Vpp without calibration) 3 digits, < ± (0.07% of amplitude range), <1mV	
Vocm (Output common mode voltage) Range Resolution, 50 Ohm load	-0.9 V to 0.9V Open, -0.45V to 0.45V@50 Ω load <10mV	
Rise/fall time (10% to 90%)	340 ps (Pulse at 0.5 Vp-p S.E.)	
Bandwidth (0.35/Trise)	1 GHz, typical (calculated)	
Analog Bandwidth , -2 dBm (sine wave at 0.5 Vpp)	1 GHz (compensating for DAC sin(x)/x roll-off), typical	
Analog Bandwidth , +3 dBm (-1dBfs) (sine wave at 0.9 Vpp)	750 MHz (compensating for DAC sin(x)/x roll-off), typical 550 MHz (not compensating for DAC sin(x)/x roll-off), typical	
Overshoot	Less than 5% (at 0.5Vp-p)	
Random Jitter on clock pattern , typ	<5 ps	
SFDR (including Harmonics)² @ 2GS/s, typical Sine Wave (62.5001 MHz) Sine Wave (125.0002 MHz) Sine Wave (250.0004 MHz)	S.E. (DC to 800MHz) -67 dBc, 0.5Vp-p -66 dBc, 0.5p-p -57 dBc, 0.5p-p	Diff. (DC to 800MHz) -71 dBc, 1Vp-p -66 dBc, 1Vp-p -58 dBc, 1Vp-p
Non Harmonic Distortion , typical	-79 dBc, 1Vp-p, DC to 800 MHz	

¹ Gain, offset, Vocm calibrated

² Waveforms were generated using DDS (Direct Digital Synthesis) with a waveform table size of 2048 samples and a phase accumulator of 32 bits. Long, non-repetitive, waveforms such as modulated or DDS (Direct Digital Synthesis)-based signals offer better spurious performance.

For periodic waveforms represented by a small number of unique samples, DAC nonlinearities limit dynamic specifications. SFDR performance may be worse at signal frequencies near to integer submultiples of the sampling frequency due to harmonic stacking on images (ex. F_s/N with $N=8,16,32$).



AT-1212 FlexRIO Adapter Module

Specifications									
Number of Analog Channels	2								
DAC Resolution	14 Bit								
Sampling Rate	1.25 GS/s								
DC-coupled analog output									
Characteristics	DC Amplified Output								
Output type	Single ended or differential								
Impedance	50 Ω / 100 Ω								
Amplitude¹ , 50 Ω Load (1KHz sine wave) Full Scale Range, Single Ended Full Scale Range, Differential Resolution	2 Vp-p (2.2Vpp without calibration) 4 Vp-p (4.4Vpp without calibration) 3 digits, < ± (0.07% of amplitude range), <1mV								
Vocm (Output common mode voltage) Range Resolution, 50 Ohm load	-1.6V to 1.6V Open, -0.8V to 0.8V@50 Ω load <5mV								
Channel-to-channel Skew, typ @1.25GS/s	50 ps								
Rise time (10% to 90%)	500 ps (Pulse at 1 Vp-p S.E.)								
Fall time (10% to 90%)	550 ps (Pulse at 1 Vp-p S.E.)								
Bandwidth (0.35/Trise)	700 MHz, typical (calculated)								
Analog Bandwidth ,+4dBm (sine wave at 1 Vpp)	650 MHz (compensating for DAC sin(x)/x roll-off), typical								
Analog Bandwidth , +9dBm (-1dBFS) (sine wave at 1.8 Vpp)	500 MHz (compensating for DAC sin(x)/x roll-off), typical 400 MHz (not compensating for DAC sin(x)/x roll-off), typical								
Overshoot	Less than 5% (at 1Vp-p)								
Random Jitter on clock pattern , typ	<5 ps								
SFDR (including Harmonics) @ 1.25GS/s, typical ² Sine Wave (39.0626 MHz) Sine Wave (78.1252 MHz) Sine Wave (156.2504 MHz)	<table style="width: 100%; border: none;"> <tr> <td style="width: 50%; text-align: center;">S.E. (DC to 480MHz)</td> <td style="width: 50%; text-align: center;">Diff. (DC to 480MHz)</td> </tr> <tr> <td style="text-align: center;">-71 dBc, 1Vp-p</td> <td style="text-align: center;">-69 dBc, 2Vp-p</td> </tr> <tr> <td style="text-align: center;">-57 dBc, 1Vp-p</td> <td style="text-align: center;">-67 dBc, 2Vp-p</td> </tr> <tr> <td style="text-align: center;">-44 dBc, 1Vp-p</td> <td style="text-align: center;">-58dBc, 2Vp-p</td> </tr> </table>	S.E. (DC to 480MHz)	Diff. (DC to 480MHz)	-71 dBc, 1Vp-p	-69 dBc, 2Vp-p	-57 dBc, 1Vp-p	-67 dBc, 2Vp-p	-44 dBc, 1Vp-p	-58dBc, 2Vp-p
S.E. (DC to 480MHz)	Diff. (DC to 480MHz)								
-71 dBc, 1Vp-p	-69 dBc, 2Vp-p								
-57 dBc, 1Vp-p	-67 dBc, 2Vp-p								
-44 dBc, 1Vp-p	-58dBc, 2Vp-p								
Non Harmonic Distortion , typical	-77 dBc, 1Vp-p, DC to 480 MHz								

¹ Gain,offset,Vocm calibrated

² Waveforms were generated using DDS (Direct Digital Synthesis) with a waveform table size of 2048 samples and a phase accumulator of 32 bits. Long, non-repetitive, waveforms such as modulated or DDS (Direct Digital Synthesis)-based signals offer better spurious performance.

For periodic waveforms represented by a small number of unique samples, DAC nonlinearities limit dynamic specifications. SFDR performance may be worse at signal frequencies near to integer submultiples of the sampling frequency due to harmonic stacking on images (ex. Fs/N with N=8,16,32).



SPECIFICATIONS

Phase noise	10 MHz	39.0625 MHz (32 points waveform)	110 MHz
Internal clock, typical			
1 KHz offset	-128 dBc/Hz	-116 dBc/Hz	-107 dBc/Hz
10 KHz offset	-136 dBc/Hz	-127 dBc/Hz	-118 dBc/Hz
100 KHz offset	-148 dBc/Hz	-139 dBc/Hz	-130 dBc/Hz
1 MHz offset	-153 dBc/Hz	-152 dBc/Hz	-151 dBc/Hz

AO 0+ / AO 0- / AO 1+ / AO 1-	DC Amplified Output
Output connector	SMA
Output impedance	50Ω S.E. / 100Ω Diff.
Io max @ 50 Ohm load	44 mA
External Clock IN	
Input connector	SMA
Input Voltage Range	-10 dBm to 8 dBm
Impedance	50 Ω, AC Coupled
Frequency range	1.25 GHz (within ±0.1%)
Damage Level	+14 dBm MAX ±25VDC MAX
External Trigger Input	
Input connector	SMA
Max data rate	140 Mbps
Input impedance	100K Ω
Trigger Level VIH min VIL max	1.75V 0.75V
Damage level	VINmax < 6.5 V VINmin > -0.5V
Slope	Rising Edge or Falling
External Trigger Output	
Output connector	SMA
Output level	3.3V open, 1.65V with 50 Ohm load
Output impedance	50 Ohm nominal

- *Typical* values describe useful product performance beyond specifications that are not covered by warranty and do not include guardbands for measurement uncertainty or drift. Typical values may not be verified on all units shipped from the factory.
- Unless otherwise noted, typical values cover the expected performance of units over ambient temperature ranges of 23 °C ± 5 °C with a 95% confidence level and humidity < 50%, based on measurements taken during development or production.
- Specifications are subject to change without notice. For the most recent specifications, visit www.activetechnologies.it



SPECIFICATIONS

Phase noise			
Internal clock, typical	10 MHz	62.5 MHz (32 points waveform)	110 MHz
1 KHz offset	-126 dBc/Hz	-110 dBc/Hz	-107 dBc/Hz
10 KHz offset	-137 dBc/Hz	-123 dBc/Hz	-118 dBc/Hz
100 KHz offset	-148 dBc/Hz	-137 dBc/Hz	-131 dBc/Hz
1 MHz offset	-154 dBc/Hz	-153 dBc/Hz	-152 dBc/Hz
AO 0+ / AO 0-	DC Output		
Output connector	SMA		
Output impedance	50Ω S.E. / 100Ω Diff.		
Io max @ 50 Ohm load	22 mA		
External Clock IN			
Input connector	SMA		
Input Voltage Range	-10 dBm to 8 dBm		
Impedance	50 Ω, AC Coupled		
Frequency	2 GHz (within ±0.1%)		
Damage Level	+14 dBm MAX ±25VDC MAX		
External Trigger Input			
Input connector	SMA		
Max data rate	140 Mbps		
Input impedance	100K Ω		
Trigger Level			
VIH min	1.75V		
VIL max	0.75V		
Damage level	VINmax < 6.5 V VINmin > -0.5V		
Slope	Rising Edge or Falling		
External Trigger Output			
Output connector	SMA		
Output level	3.3V open, 1.65V with 50 Ohm load		
Output impedance	50 Ohm nominal		

- *Typical* values describe useful product performance beyond specifications that are not covered by warranty and do not include guardbands for measurement uncertainty or drift. Typical values may not be verified on all units shipped from the factory.
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